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EXAMINER	
WHIPKEY, JASON T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,333	SU ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-13* is/are rejected.

7)☒ Claim(s) *5,6 and 14-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 18, 2007, have been fully considered but they are not persuasive.

Regarding claim 1, on page 17, Applicant argues, "Bock does not teach an integrator circuit with a switch to control the voltage value of the electronic signal periodically in a reset voltage and in a bright voltage." This assertion is incorrect. Bock discloses that pixel sensor 50 (an integrator circuit) has a reset transistor M1 (a switch). As described in paragraph 22, the pixel outputs a signal when the reset switch is on (a reset voltage) and when the reset switch is off (a bright voltage).

Also on page 17, Applicant argues, "the Bock reference does not generate an output signal having a voltage value which is the difference between the reset voltage and the bright voltage in order to eliminate noise." This assertion is also incorrect. Bock discloses in paragraph 22 that correlated double sampling (CDS) is performed. CDS is a process that inherently calculates the difference between a pixel signal when a reset switch is off (a bright voltage) and a pixel signal when a reset switch is on (a reset voltage).

On page 18, Applicant argues, that the Mizuno reference does not teach or allude to the correlated double sampling circuit that operates as recited in claim 1. However, the revised rejection below shows that Applicant's assertion is incorrect.

Specification

2. The amendment to the specification is approved and the corresponding objection is withdrawn.

Claim Objections

3. The amendment to the claims has overcome the claim objections. The objections are withdrawn.

4. Claims 1-16 are objected to because claim 1 recites "adopting in CMOS process" on line 2, which is unclear. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 10 recites "a CMOS transistor". There is no accepted definition for this term, as a CMOS device comprises a number of transistors.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 11, 12, and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 11 recites the limitation "the charge storing device" on line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the reference voltage" on line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the CMOS switch" on line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the inverter" on lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Bock (U.S. Patent Application Publication No. 2002/0033439).

Regarding **claim 1**, Bock discloses an integrated image detecting apparatus (see Figure 3) adopting in CMOS process (see paragraph 17), comprising:

an optical detecting element (photodiode 60) detecting an optical variation and converting photons into charge (see paragraph 20);

an integrator circuit (pixel sensor 50) converting charge produced by the optical detecting element into an electronic signal (inherently performed by source-follower transistor M2; see paragraph 21), wherein the integrator circuit comprises a switch (reset transistor M1) to control the voltage value of the electronic signal periodically in a reset voltage (a reset level is output from the pixel when the RST signal is high; see paragraph 22), defined as a voltage when said switch is in an "on" condition, and in a bright voltage (a regular pixel signal is output when the RST signal is low; see paragraph 22), defined as a voltage when said switch is in an "off" condition, said reset voltage and said bright voltage having differing values (high and low, respectively);

a correlated double sampling circuit (comprised of transistors M9 and M10 and capacitors C_1 and C_2) connecting to the integrator circuit for reading the electronic signal output from the integrator circuit, and generating an output

signal with a voltage value of the difference between the reset voltage and the bright voltage periodically following the operation of the switch of the integrator circuit (see paragraph 22); and

an output circuit (readout circuit 52), receives the output signal of the correlated double sampling circuit and outputs a plurality of signals (70 and 72; see paragraph 22).

Regarding **claim 9**, Bock discloses:

the electronic signal is in the reset voltage while the switch inside the integrator circuit turns on, and the electronic signal is in the bright voltage while the switch inside the integrator circuit turns off (see paragraph 22).

Regarding **claim 10**, Bock discloses:

the switch is a transistor selected from the group consisting of an NMOS transistor (see paragraph 20), a PMOS transistor, and a CMOS transistor.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claims 1, 3, 4, 7, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno (U.S. Patent Application Publication No. 2002/0190193) in view of Ikeda (U.S. Patent No. 6,111,606).

Regarding **claim 1**, Mizuno discloses an integrated image detecting apparatus (see Figure 6), adopting in CMOS process, comprising:

an optical detecting element (photodiode PD), detecting an optical variation and converting photons into charge (see paragraph 39);

an integrator circuit (integrator circuit 10; see paragraph 87), converting charge produced by the optical detecting element into an electronic signal (see paragraphs 43 and 97), wherein the integrator circuit comprises a switch (SW_{11}) to control the voltage value of the electronic signal periodically in a reset voltage (see paragraph 61), defined as a voltage when said switch is in an "on" condition, and in a bright voltage, defined as a voltage when said switch is in an "off"

condition, said reset voltage and said bright voltage having differing values (see paragraph 63);

a correlated double sampling circuit (20) connecting to the integrator circuit for reading the electronic signal output from the integrator circuit, and generating an output signal with a voltage value of the difference between the reset voltage and the bright voltage periodically following the operation of the switch of the integrator circuit (see paragraphs 84-87); and

an output circuit (sample and hold circuit 30) performs the output signal of the correlated double sampling circuit (see paragraph 88).

Mizuno is silent with regard to outputting a plurality of signals.

Ikeda discloses a signal processor for an imaging device (see Figure 9), wherein sample-and-hold circuit components 69 and 70 each output a signal.

An advantage of outputting two signals is that a slower sample-and-hold circuit can be used, thereby reducing the need for more expensive high-speed components. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system output a plurality of signals.

Regarding **claim 3**, Mizuno discloses:

the integrator circuit further comprises an operational amplifier (A_1; see Figure 6) connecting to the optical detecting element for receiving charge produced by the optical detecting element and outputting the electronic signal (see paragraphs 73 and 74), and the switch is connected between the input terminal and the output terminal of the operational amplifier (see Figure 6) which the

switch is turned on and off periodically for controlling the voltage value of the electronic signal periodically in the reset voltage and in the bright voltage (see paragraphs 73 and 74).

Regarding **claims 4 and 8**, Ikeda discloses:

the unit gain operational amplifier is a single stage amplifier (see Figure 9).

Ikeda is silent with regard to the type of transistors that comprise the operational amplifier.

Official Notice is taken that it was well known in the art at the time the invention was made to use NMOS and/or PMOS transistors in an operational amplifier. An advantage of doing so is that the resulting operational amplifier requires less power and produces lower noise. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Mizuno's system use NMOS or PMOS transistors in an operational amplifier.

Regarding **claim 7**, Ikeda discloses:

the output circuit comprises a sample and a hold circuit (69 and 70; see column 11, lines 11-15) and a plurality of unit gain operational amplifiers (operational amplifiers 75 and 76 are used as buffers, which inherently have a gain of unity; see column 12, lines 30-31).

Regarding **claim 11**, see the rejection under 35 U.S.C. 112, second paragraph, *supra* and note that several capacitors are shown in Figure 6.

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno in view of Ikeda and further in view of Wang (U.S. Patent No. 6,518,085).

Claim 2 can be treated like claim 1. However, Mizuno is silent with regard to the construction details of the photodiode.

Wang discloses a CMOS imager, wherein:

> the optical detecting element is a photodiode adopting N-sub or P-sub of CMOS process (see column 4, lines 33-39).

As described in column 4, lines 33-39, an advantage of using such a photodiode is that it has a uniform spectral response. For this reason, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Wang's system include a photodiode adopting "N-sub or P-sub of CMOS process".

Allowable Subject Matter

15. Claims 5, 6, and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding each of these claims, no prior art could be located that teaches or fairly suggests an integrated image detecting apparatus, including an optical detecting element, integrator circuit, and correlated double sampling circuit, wherein the correlated double sampling circuit comprises an AC couple device, a CMOS switch, and a unit gain operational amplifier, wherein the AC couple device is connected between the integrator circuit and the unit gain

operational amplifier and the CMOS switch is connected between a reference voltage source and the transmission path of the AC couple device and the unit gain operational amplifier.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Whipkey, whose telephone number is (571) 272-7321. The examiner can normally be reached Monday through Friday from 9:30 A.M. to 6 P.M. eastern standard time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye, can be reached at (571) 272-7372. The fax phone number for the organization where this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JTW

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January 6, 2008

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SUPERVISORY PATENT EXAMINER